AN EASY-TO-USE FET DRO DESIGN PROCEDURE SUITED TO MOST CAD PROGRAMS

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ABSTRACT

A design procedure for a reflection stabilised dielectric resonator oscillator (DRO) is given that takes advantage of the facilities available from most linear microwave CAD programs, hence streamlining and simplifying the task. 27.61GHz MESFET hybrid DROs were designed using this method. These DROs gave an average output power of +3dBm, with +/-2MHz stability from -20 to +40°C and -75dBc/Hz phase noise at 10 kHz from carrier.

INTRODUCTION

A 27.61GHz FET DRO was required as the local oscillator in a receiver downconverter [1], to have an output power >+3dBm, a high frequency stability and low phase noise, and yet have the potential for low cost. At the start of the design the authors found the oscillator discussions in reference books to be rather general and not fully exploiting the benefits of CAD. Recently, interesting papers [e.g., 2,3] have been published concerning the use of CAD as an aid to oscillator circuit design, including optimisation. However, these techniques use specialised programs, not available to the authors during our design, and are probably not yet commonplace within other microwave design facilities. The design approach given here does not involve the same rigorous optimisation as described in [2,3], but allows working oscillators to be designed successfully in a very short time, using a linear analysis software tool of the type found in most microwave laboratories. Additionally, advantage is taken of the speed, number-crunching power and user interface (especially tables of results and Smith charts) provided by these commercial microwave CAD programs, so giving a fast turnaround time and adding an extra dimension of insight into important aspects such as the stability of oscillations.

This easy to understand procedure for designing reflection stabilised oscillators does not require any complicated formulae or mapping, and is applied here to a series feedback reflection stabilised DRO at 27.61GHz. This oscillator type was chosen for several good reasons: DR feedback stabilisation may be too lossy at this frequency to promote oscillation; absorption or transmission oscillators give lower output powers due to the loss in the resonator on the output; and the reflection oscillator has superior frequency stability and pulling performance due to the isolation of the frequency determining element from the output. Another consideration is that easily obtainable 2-port S-parameters can be used without the added complexity of converting to 3-port S-parameters, sometimes required for parallel feedback.

MODELLING

Firstly, this design procedure is followed using a small-signal model for the FET. This allows the circuit to be designed to ensure start-up and stable oscillations, and also allows the oscillation frequency, F_{osc}, to be set approximately. The device chosen was an NE67300 chip MESFET with a 0.3 micron gate length. As S-parameters for this were not available at 27.61GHz, measurements were made to 20GHz, and the equivalent circuit model fitted to these was used to generate an S-parameter data file for the higher frequency range. Measurements must be carried out at the dc bias point chosen for the oscillator, not taken from data sheets.

There are advantages to be gained from additionally deriving a non-linear FET model:

1) The S-parameter dependence on bias can be observed, so that the optimum bias can be estimated.
2) The model can be incorporated into a non-linear simulation program.
3) Amplitude dependent S parameters can be obtained. After the circuit is designed using small signal S-parameters, these large-signal S-parameters may be used in the design procedure to refine certain aspects such as maximum negative resistance and the correct F_{osc}.

Five stages were involved in obtaining a large-signal model and consequently the large signal S-parameters:

1) measure the FET S-parameters at six bias points,
2) derive a non linear FET model using the non-linear equivalent circuit modelling program SOPTIM [4],
3) incorporate this user model into the time domain simulation program ANAMIC [4],
4) run ANAMIC with large amplitude sinewaves applied to the FET, biased realistically, in a certain sequence, and
5) carry out a Fourier analysis on the input and output waveforms and derive S-parameters from the fundamental frequency components.

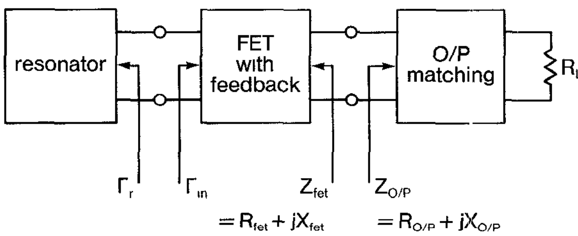

Figure 1. Oscillator model

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DESIGN PROCEDURE

The block schematic of a reflection stabilised oscillator is shown in Figure 1. Steps 1 to 7 below make use of any linear CAD program such as TOUCHSTONE™.

Step 1) Design the 'FET with feedback' sub-circuit shown in Figure 1. Feedback is applied to the FET, and optimised for maximum negative resistance, R_{fet}.

Step 2) Plot the input and output stability circles of this block at F_{osc}.

Γ_r and $Z_{o/p}$ must lie in the potentially unstable areas on the Smith chart to obtain negative resistance at both ports. *...Rule 1*

Step 3) Design a resonator circuit with Γ_r according to rule 1.

For start-up $$|\Gamma_r| > \frac{1}{|\Gamma_{in}|} \quad \text{...Rule 2}$$

and $$\arg(\Gamma_r) = \arg\left[\frac{1}{\Gamma_{in}}\right] \quad \text{...Rule 3}$$

Therefore, if the resonator has a high Q, it will control the oscillator frequency. After start-up $1/\Gamma_{in}$ will increase until $1/\Gamma_{in} = \Gamma_r$. $|\Gamma_r|$ should be as high as possible.

Step 4) Design the output matching circuit to transform R_L to $Z_{o/p}$ given by:

$$R_{o/p} + j\,X_{o/p} = -\frac{R_{fet}}{3} - j\,X_{fet} \quad \text{...Rule 4}$$

After start-up the negative resistance R_{fet} will decrease until $R_{fet} = -R_{o/p}$. Rule 4 gives maximum power transfer to the load assuming that the magnitude of the negative conductance decreases linearly with increasing amplitude [5]. This approximation has been found to give good results in practice.

Step 5) $1/\Gamma_{in}$ changes with $Z_{o/p}$, so it is now necessary to iteratively repeat steps 3) and 4) a few times until Rules 1 to 4 are met simultaneously. This simply involves using the 'tune' facility to adjust the resonator and output circuit.

Step 6) Test for oscillator stability at frequencies close to F_{osc} [6] by displaying $1/\Gamma_{in}$ and Γ_r on a Smith chart. $1/\Gamma_{in}(f)$ and $\Gamma_r(f)$ should pass in opposite directions on the Smith chart, to ensure that the above conditions for oscillation apply at only one spot frequency. *...Rule 5*

Step 7) Check that the oscillation conditions do not occur at any frequency other than F_{osc}, from near DC to as high in frequency as the simulator can be trusted, in order to complete this stability analysis. This is best done by checking through a table of reflection coefficients and impedances. *...Rule 6*

Step 8) (Optional) If a non-linear model has been derived, then the oscillator can be simulated by a non-linear analysis program. This checks frequency and output power.

It is also possible to use such a program to plot the predicted $1/\Gamma_{in}$ dependency upon amplitude and identify the angle of intersection between $1/\Gamma_{in}(v,f)$ and $\Gamma_r(f)$ on the Smith chart. This should be 90° to minimise AM to PM noise conversion [6]. Although this is computationally intensive, it is more practical than measurements at 27.61GHz.

PRACTICAL DESIGN EXAMPLE

The circuit of the series feedback reflection stabilised DRO is shown in Figure 2. The following are the steps taken to design this circuit:

Step 1) The model of the FET is in the form of an S-parameter data file, and series feedback is added by a reactance in the common (source) lead. This is provided in this case by the source bias filter, and at this step the length 'a' is optimised.

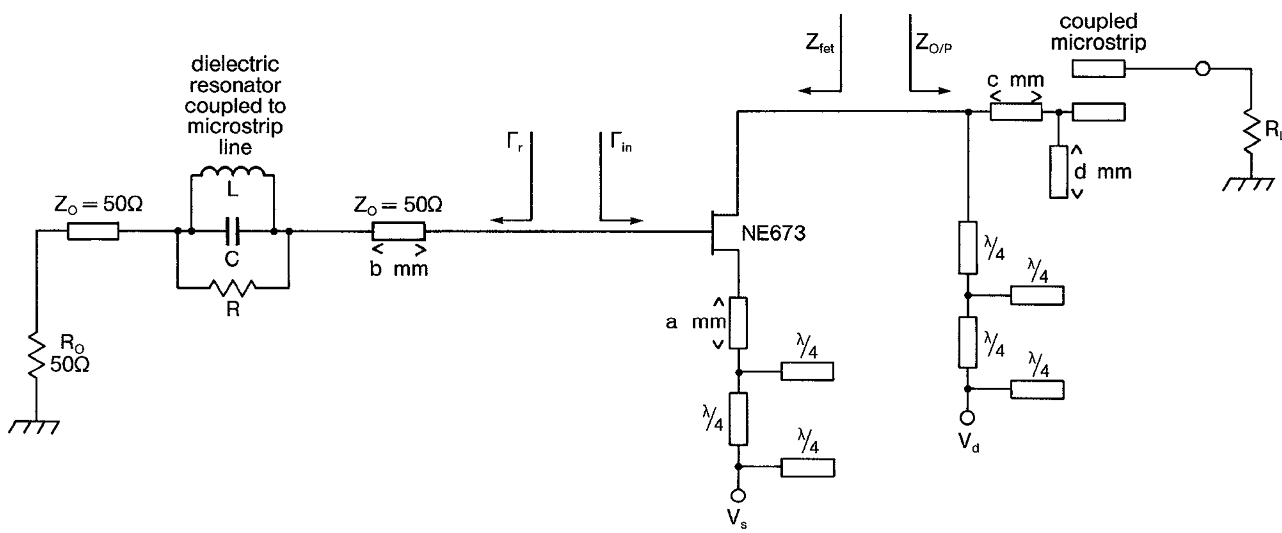


Figure 2. Circuit of DRO

Step 2) The stability circles of the FET with feedback are plotted in Figure 3. The shaded region represents stability, so $Z_{o/p}$ and Γ_r must lie between the stability circles and the perimeter of the Smith chart.

Step 3) The dielectric resonator, DR, coupled to a microstrip line is modelled by a parallel LCR circuit in series with the matched gate line. The unloaded Q and the coupling are chosen to meet Rule 2, and the length 'b' adjusted to meet Rule 3.

Step 4) The output circuit is designed to meet Rule 4 by optimising lengths 'c' and 'd'.

Step 6) Figure 4 shows a plot of $1/\Gamma_{in}$ and Γ_r from 25GHz to 29GHz. It can be seen that the trajectories are opposite and parallel in the region of F_{osc} – the ideal situation.

Step 7) Figure 5 shows the results table produced by TOUCHSTONE™. It can be seen that rules 1-4 are met at 27.61GHz, but not at any other frequency, hence stable oscillations are predicted.

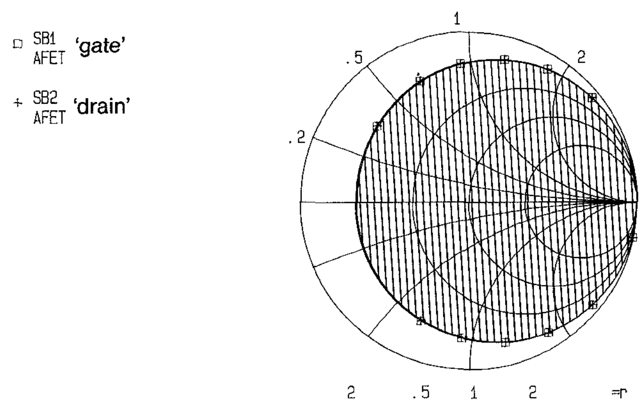


Figure 3. Stability circles at the FET gate and drain ports, with feedback

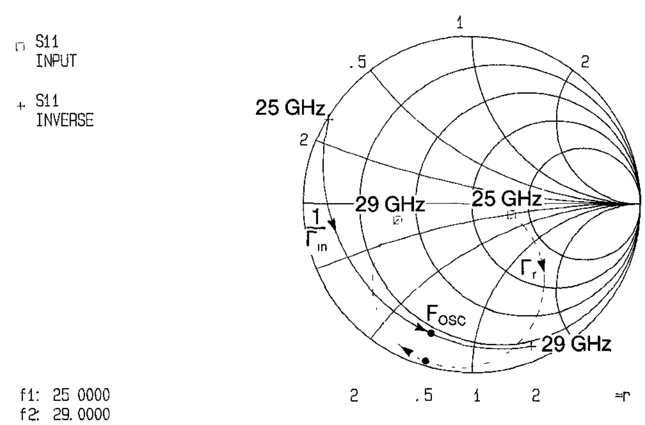
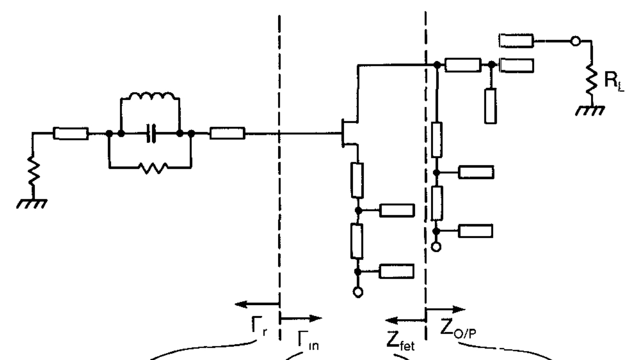


Figure 4. Plot of $\frac{1}{\Gamma_{in}}$ and Γ_r near F_{osc}

The circuit is fabricated in microstrip on an alumina substrate and includes a thin-film nichrome 50Ω resistor, R_o. A photograph of the assembled oscillator is shown in Figure 6. The dielectric resonator is fabricated from Murata U-type material with a dielectric constant of 38.6.

The required temperature coefficient, T_f, of the DR was identified by temperature cycling the DRO with a 0ppm/°C DR. The oscillator then exhibited a drift of -10ppm/°C. The DRO was temperature cycled in a test fixture with two different DRs of T_f = +4ppm/°C and +8ppm/°C, respectively. The results are shown in Figure 7. The DRO fitted with the DR of T_f = +8ppm/°C exhibited a frequency drift within +/-0.5MHz from -20 to +40°C and was therefore chosen for the final version.



freq (GHz)	$\lvert\Gamma_r\rvert$	$\angle\Gamma_r$	$\left\lvert\frac{1}{\Gamma_{in}}\right\rvert$	$\angle\frac{1}{\Gamma_{in}}$	R_{fet}	X_{fet}	$R_{O/P}$	$X_{O/P}$
1.00000	0.002	86.278	1.041	5.552	639.206	495.944	31.914	29.765
2.00000	0.003	82.538	1.032	5.499	641.664	-1.6e+03	52.009	5.265
3.00000	0.005	78.815	0.943	8.428	-122.200	-534.429	38.317	-8.952
4.00000	0.008	75.080	0 824	14.272	-99.160	-244.703	23.791	-6.171
5.00000	0.009	71.336	0.653	25.161	-44.705	-118.046	13 590	3.716
6 00000	0.011	67.605	0.459	64.924	12.617	-58.199	6.030	18.972
7.00000	0.014	63.839	0.940	106.829	59.401	-42.661	0.513	45.722
8.00000	0.016	60 083	1.446	132.979	85.695	-50.219	19 529	117.809
9.00000	0.018	56.325	12.278	-175.818	91.571	-64 171	191.524	-4 284
10 0000	0.021	52.550	4.056	20.584	84.401	-73.870	70.295	-35.140
11.0000	0.024	48.770	2.495	39.368	70.541	-77.307	44.053	-14.697
12.0000	0.027	44.941	1.931	58.366	55.187	-75.266	35.559	0.897
13.0000	0.030	41.138	1.438	84 330	36 159	-69.144	33.170	15 636
14.0000	0.034	37.274	0.743	135.550	7.954	-51.359	35.706	34.973
15.0000	0.039	33.393	2.546	-140 180	24.367	0.536	60.024	94.155
16.0000	0.044	29.467	31.927	-118.777	39.904	-9.232	10.642	-37.443
17.0000	0.050	25.500	1.635	-151.818	35.402	-7.906	26.874	19 868
18.0000	0.057	21.463	1.300	-109 864	32.161	-0 848	39.575	44 484
19.0000	0.065	17.339	1.258	-81.757	29.758	7.560	60.704	68.134
20.0000	0 076	13.087	1.282	-60.698	29.304	16.900	106 297	91.967
21.0000	0.090	8.636	1.331	-43.064	29.641	25.940	208.893	74 862
22 0000	0.109	3.938	1.402	-25.098	31.565	35.225	213.649	-101.768
23.0000	0 135	-1.255	1.508	-2.395	35 430	43 975	103.770	-155 389
24.0000	0.176	-7.275	1.637	34.947	42.168	52.164	40.125	-117.828
25.0000	0.244	-15.007	1.433	104.159	54.185	56 412	17.879	-86.384
26.0000	0.385	-27.319	0.936	-172.630	74.904	41.902	8.776	-64.653
27 0000	0.743	-57 070	0.838	-118.682	20.275	-5.303	4.477	-48.925
27.6000	0 980	-100.003	0.854	-99.412	-8.860	41.309	2.972	-41 310
28.0000	0.854	-130.889	0.870	-89.863	-4.487	64.265	2 235	-36.771
29.0000	0 449	-167.822	0 910	-73.629	14 206	93.814	1.002	-26.794
30.0000	0.287	178.305	0.943	-62.165	32.743	112.210	0.334	-18.157

rule 2 ($\lvert\Gamma_r\rvert$ 0 980 and $\left\lvert\frac{1}{\Gamma_{in}}\right\rvert$ 0.854, at 27.6000); rule 3 ($\angle\Gamma_r$ -100.003 and $\angle\frac{1}{\Gamma_{in}}$ -99.412, at 27.6000); rule 4 (R_{fet}, X_{fet}, $R_{O/P}$, $X_{O/P}$, at 27.6000)

Figure 5. DRO equivalent circuit and TOUCHSTONE printout

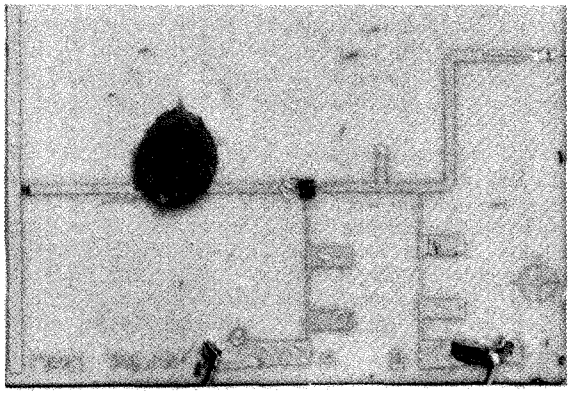


Figure 6. Photograph of hybrid DRO

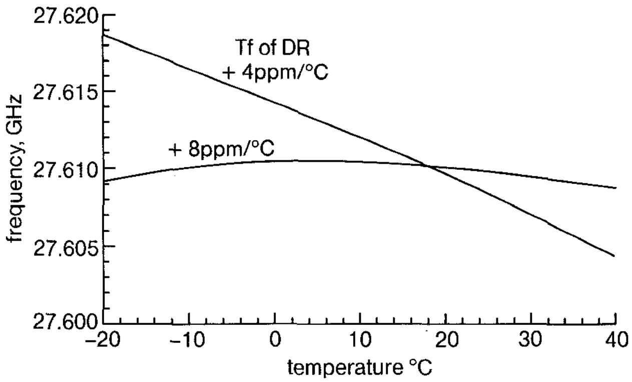


Figure 7. Frequency stability of DRO in text fixture with two DRs of differing temperature coefficients

RESULTS

Eight DROs have been made, and Figure 8 shows the range of powers obtained. Typical output power is in excess of +3dBm. Phase noise is -75dBc/Hz at 10kHz off-carrier, as shown in Figure 9. When placed in the receiver housing the frequency stability was an acceptable +/-2MHz from -20 to +40°C.

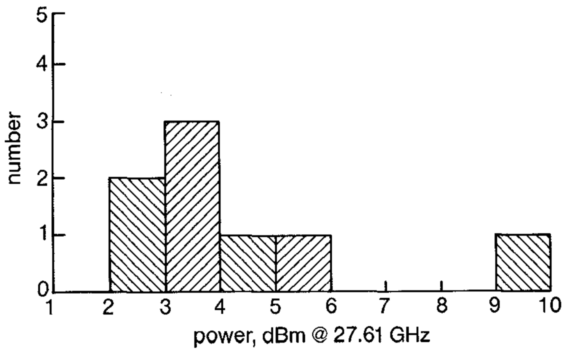


Figure 8. Powers obtained from 8 oscillators

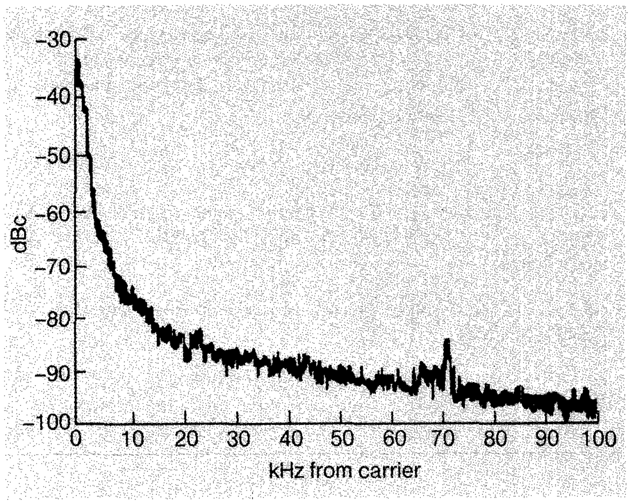


Figure 9. DRO noise spectrum

CONCLUSIONS

A simple set of design rules for a reflection stabilised oscillator has been presented, compatible with established linear microwave CAD programs. This oscillator design procedure does not predict nor optimise the output power or noise spectrum, yet it has been shown here to have successfully designed a millimetre-wave DRO exceeding our specifications. The strength of the method lies in its simplicity, speed and intuitive feel. In order to take greater advantage of the FET saturated output power capability a device with higher gain is required, e.g. a HEMT. The circuit has been designed to be transferable to GaAs with few modifications, consistent with our aim of complete monolithic integration of a millimetre-wave receiver downconverter.

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